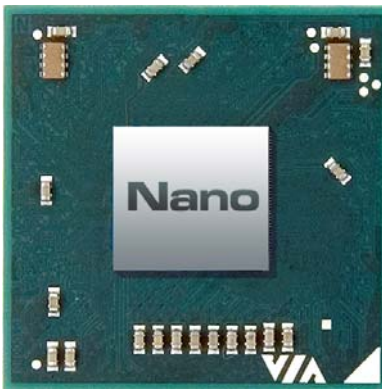




VIA Nano™ Processor



Introductory White Paper

VIA Technologies, Inc.
May 2008



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1. Introduction to the VIA Nano™ Processor

The last few years have seen significant changes within the microprocessor industry, and indeed the entire IT landscape. Much of this change has been driven by three factors: the increasing focus of both business and consumer on energy efficiency, the rise of mobile computing, and the growing performance requirements of computing devices in a fast expanding multimedia environment.

In the microprocessor space, the traditional race for ever faster processing speeds has given way to one that factors in the energy used to achieve those speeds. Performance per watt is the new metric by which quality is measured, with all the major players endeavoring to increase the performance capabilities of their products, while reducing the amount of energy that they require.

Based on the recently announced VIA Isaiah Architecture, the new VIA Nano™ processor is a next-generation x86 processor that sets the standard in power efficiency for tomorrow's immersive internet experience. With advanced power and thermal management features helping to make it the world's most energy efficient x86 processor architecture, the VIA Nano processor also boasts ultra modern functionality, high-performance computation and media processing, and enhanced VIA PadLock™ hardware security features.

Augmenting the VIA C7® family of processors, the VIA Nano processor's pin compatibility extends the VIA processor platform portfolio, enabling OEMs to offer a wider range of products for different market segments, and furnishing them with the ability to upgrade device performance without incurring the time and cost expense associated with system redesign.

1.1 Positioning

The high performance of the VIA Nano processor, coupled with its ultra low power consumption makes it the ideal mobile computing processor. It will initially power a range of 'slim 'n' light' notebooks, fusing all of the VIA C7 processor's advantages in battery-life, size and cool operation together with the higher computational performance of the VIA Nano processor's advanced x86 architecture.

The VIA Nano processor will also appear in ultra mobile mini-note devices and small form factor, green desktop systems for home and office use.





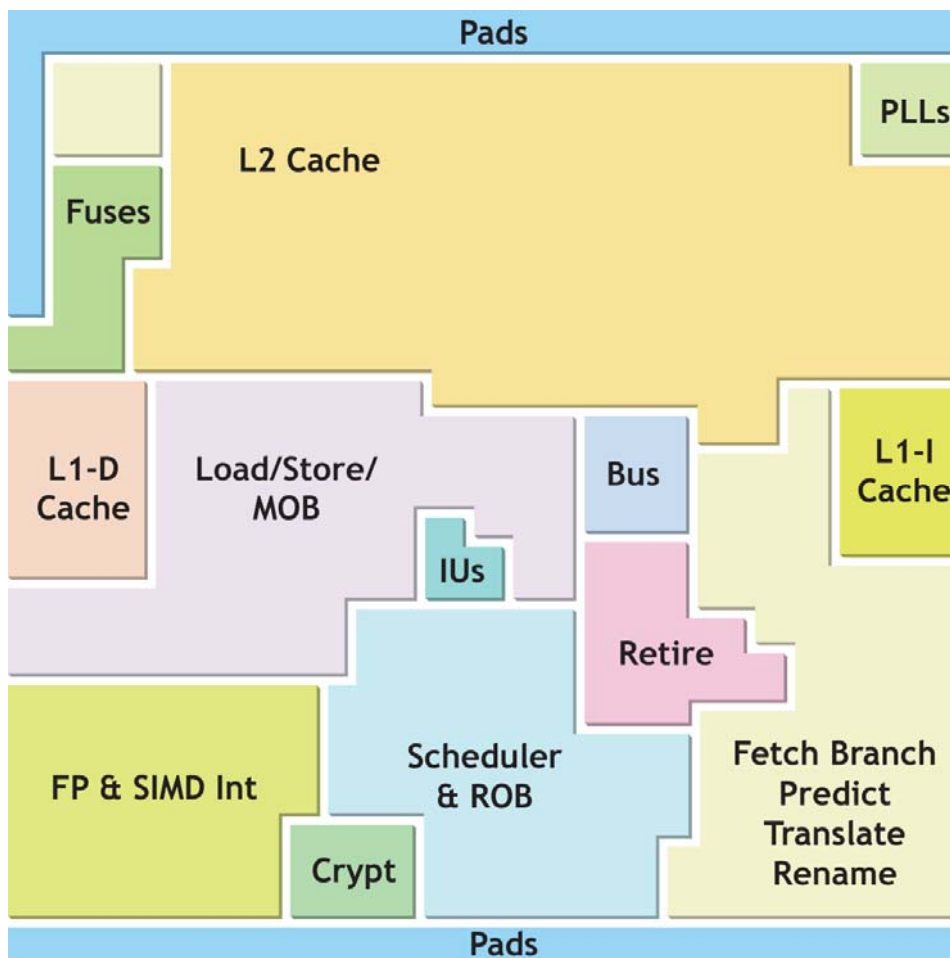
2. Key Specifications

The VIA Nano processor uses proven 65 Nanometer technology delivering the ideal blend of powerful performance and performance efficiency. With roughly twice the numbers of transistors as the 90nm-based VIA C7 processor range, the VIA Nano processor is able to offer state-of-the-art capabilities such as virtualization, advanced thermal management, and innovative security enhancements that provide the foundation for energy-efficient, feature rich computing solutions.

Underscoring VIA's leadership in processor miniaturization, the VIA Nano processor comes with ultra compact dimensions, enabling a new generation of small form factor designs and new, smaller applications for the x86 platform.

- Package size: Compact VIA NanoBGA2 package (21mm x 21mm)
- Die size: 7.650mm x 8.275mm (63.3 square mm)

Figure 1: VIA Nano Processor Block Diagram





The VIA Nano processor will initially be offered in five different skus: two “Low Voltage” versions (L2100 and L2200), and three “Ultra Low Voltage” (U2400, U2500 and U2300), as shown in Table 1:

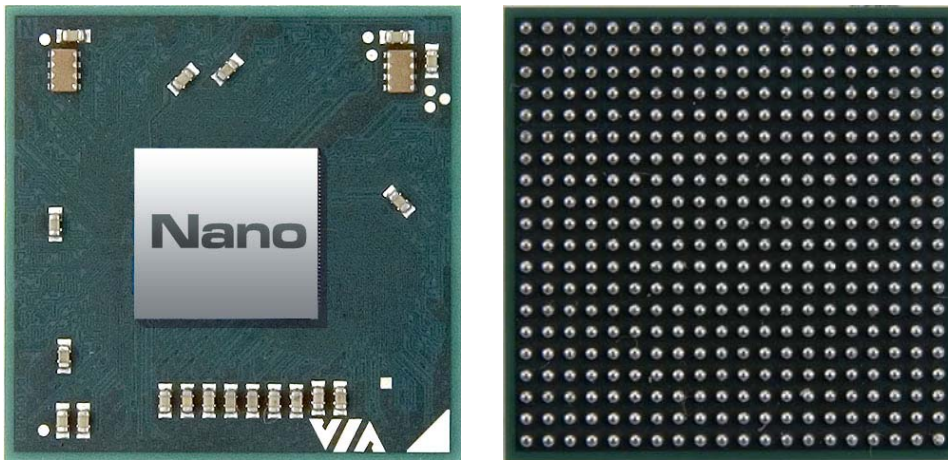
Table 1: VIA Nano Processor Initial Skus

Model No.	Frequency	FSB	TDP (max)	Idle Power	L2 Cache
L2100	1.8GHz	800MHz	25 watts	500mW	1MB
L2200	1.6GHz	800MHz	17 watts	100mW	1MB
U2400	1.3 ⁺ GHz	800MHz	8 watts	100mW	1MB
U2500	1.2GHz	800MHz	6.8 watts	100mW	1MB
U2300	1.0GHz	800MHz	5 watts	100mW	1MB

2.1 Green Technology

In addition to complying with RoHS and WEEE directives, the VIA Nano processor goes beyond mandated requirements and will be part of the first processor platform to employ halogen-free as well as lead-free packaging technology.

Figure 2: VIA Nano Processor Front and Back





3. VIA Nano Processor Technical Overview

3.1 Superscalar and Speculative Out-of-Order Architecture

The VIA Nano processor range is based on the VIA Isaiah Architecture – the first superscalar, out-of-order architecture designed by Centaur Technology, VIA's Austin, Texas-based microprocessor design team.

At a high level, all modern superscalar and out-of-order architectures are similar. Differences arise due to different product objectives, different technologies, and different design philosophies. These detailed differences lead directly to the resulting products having different levels of performance and power consumption.

The VIA Nano processor can decode three full x86 instructions per clock, generate three fused micro-ops per clock, issue (speculatively and out-of-order) seven execution micro-ops per clock to seven execution ports, and retire three fused micro-ops per clock.

Figure 2 shows a conceptual picture of the VIA Nano processor components and pipeline structure. The pipelines fetch x86 instruction bytes and translate them into internal machine instructions, called micro-ops. x86 instructions and micro-ops proceed in program order down this portion of the pipeline (“in-order”). The speculative label refers to the fact that the processor may not be actually fetching the correct program instructions (in cases of a branch misprediction, for example).

Out-of-order issue and execution happens where the pipeline components take the translated micro-ops and issue them to the appropriate execution units. The issue and execution is not necessarily in program order; instructions are issued and executed whenever their inputs are available (thus “out-of-order”). Performing out-of-order issue and execution relies on micro-ops (and their operands and results) and is maintained in a Reorder Buffer (ROB) and a Memory Reorder Buffer (MOB). The result of a micro-op execution is returned to the ROB awaiting its in-order retirement.

3.2 Advanced Branch Prediction

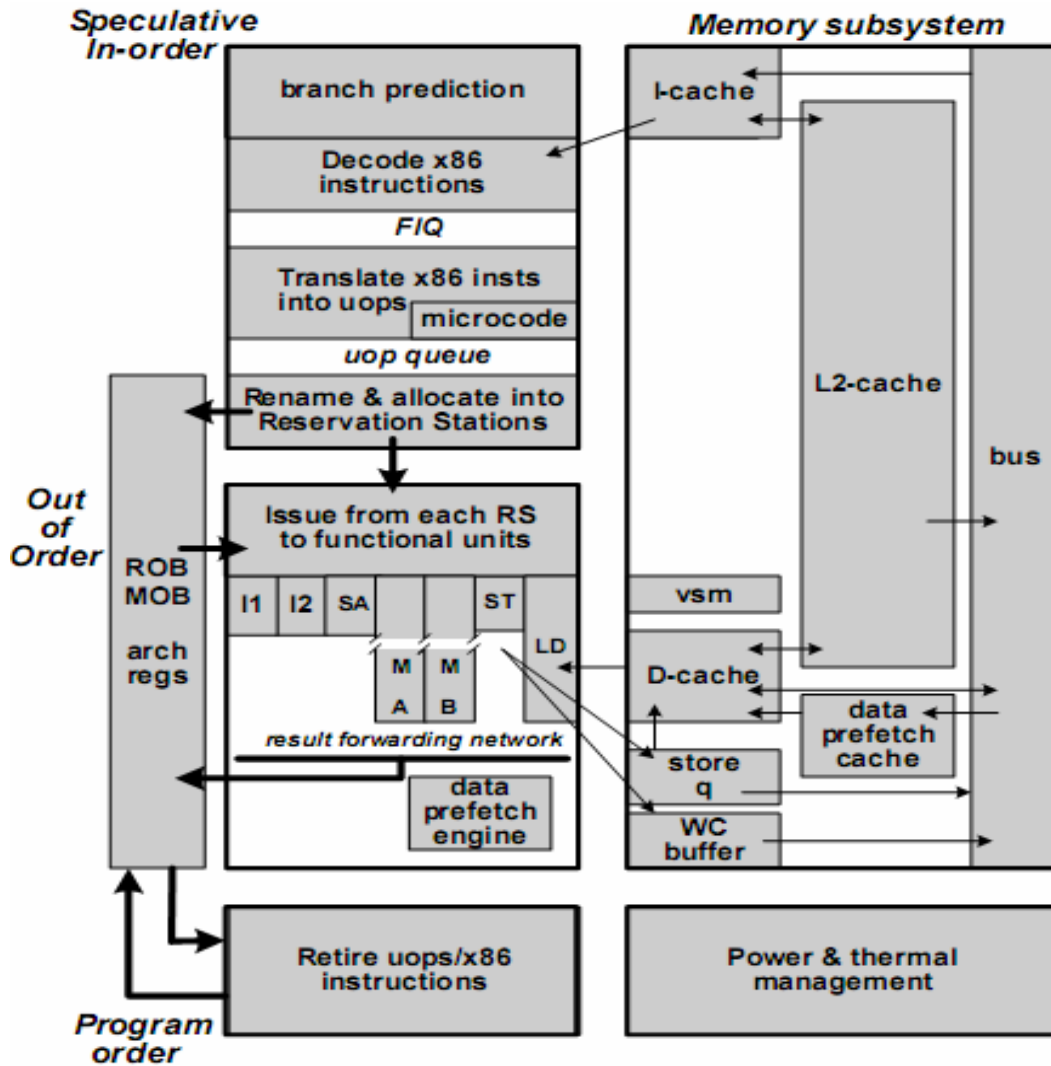
The VIA Nano processor implements a very powerful and a unique branch prediction algorithm using eight different predictors in two different pipeline stages. The first fetch pipeline stage contains three predictors of conditional branch behavior (each more accurate for a particular type of branch), a predictor of which of these predictors to use, and a separate return predictor.

The translate stage (where more information about the instructions is known) contains a return predictor, a conditional branch “overflow” predictor, and a default predictor. Each predictor is designed to be more accurate for a particular type of branch at a particular point in the pipeline. The predictors interact and “vote” to obtain the final prediction.





Figure 3: VIA Nano Processor Architecture Overview



3.3 Smart cache Subsystem

The VIA Nano processor includes many innovations in the cache subsystem that lead to very efficient use of total cache area (and thus cache power). The cache subsystem comprises the level-1 instruction cache (I-cache), the level-1 data cache (D-cache), the unified level-2 cache (L2-cache), and some specialized caches or buffers. Each of the I- and D-caches contains 64K bytes and is 16-way set associative.

The L2-cache is organized as 16-way associative and is designed to support a wide variety of sizes with minimal implementation effort. The size of the L2-cache in the



first VIA Nano processor implementation is 1 MB, but subsequent processors may have different sizes.

In addition, the L2 cache is “exclusive”, meaning that the L1 caches’ contents do not reside in our L2 cache, thus increasing the effective size of the L2 cache over the “inclusive” approach of competitor architectures.

Another feature unique to the VIA Nano processor is that many of the data-prefetch algorithms load prefetched data into a special 64-line prefetch cache as opposed to loading it directly into the L2-cache. This approach improves the efficiency of the L2 cache and the smaller size is adequate since the useful lifetime of prefetched data is short.

3.4 High Performance Media Computation

The VIA Nano processor places significant emphasis on high-performance floating-point execution. It can execute four floating-point adds and four floating-point multiplies every clock. It uses a completely new algorithm for floating-point adds that results in the lowest floating-point add latency of any x86 processor—two clocks for any format (SP, DP, DE, packed or scalar). Similarly, the floating-point multiplier has the lowest latency of any x86 processor—three clocks for SP multiply, and four for DP and DE.

In addition, the integer data path for SIMD integer (SSEx) instructions is 128-bits wide, and almost all SSEx instructions (including all shuffles) execute in only one clock.

3.4.1 Blu-ray Disc™ playback

Play-back of DVD content with any modern CPU is now straightforward, however the advent of High Definition content and the rise of the next-generation optical format, Blu-ray Disc™ technology, has brought new and far more demanding computing requirements to the PC marketplace.

The VIA Nano processor’s superscalar, out-of-order architecture facilitates exceptionally smooth play back of Blu-ray and other HD video formats, which can have encrypted media streams of up to 40Mbps.

3.4.2 Gaming

When combined with an appropriate discrete graphics card, the VIA Nano processor’s robust two-clock FPU multiply and 128 bit data path offers an excellent gaming experience, providing silky smooth rendering of 3D images.





3.5 Advanced Power and Thermal Management

In addition to VIA's usual aggressive dynamic management of active power, the VIA Nano processor utilizes new low-power circuit techniques. The latest x86 instruction-level power controls are included along with a new "C6" power state where the caches are flushed, internal state is saved, and the core voltage is turned off.

Unique to the VIA Nano processor are several new VIA Adaptive PowerSaver™ features. They include fine-grained algorithms for adaptively transitioning between performance and voltage states ("P" states) while the processor continues to run.

Yet another feature provides automatic overclocking if the die temperature is low. Another feature allows the processor to automatically maintain the die temperature at a user-specified temperature. Several other new power and thermal management features are provided.

3.5.1 VIA Adaptive PowerSaver™ Technology

Adaptive PowerSaver™ Technology is the name for a group of several P-state optimizations. When shifting the P-state between the current and a higher target state the VIA Nano processor, unlike Intel processors that stop the bus and processor execution, is able to achieve the transition whilst the bus and program execution remain running. This results in a significant improvement in responsiveness during the many P-state changes a mobile processor performs.



Another unique VIA Nano processor mechanism automatically adjusts the P-state voltage based on the die temperature. Assume, for example, that a processor normally requires 1.1V to run at 2GHz at its maximum rated die temperature. If, however, during a transition to 2GHz speed, the die temperature is 20 lower than the maximum rated, then the Adaptive P-State Control feature automatically calculates that only, say, 1.0V is needed to achieve 2GHz and accordingly only shifts to 1.0V.

Additionally, the VIA Nano processor implements an Adaptive Thermal Limit mechanism. The software system can say, for example, that it wants the die maintained no hotter than 80° (that may be all the heat the system can remove). Using this unique mechanism, the processor will automatically and dynamically adjust P-states such that the target die temperature is not exceeded.

3.5.2 Thermal Design Power

Through the above innovations in processor architecture, the VIA Nano processor is able to offer significant performance improvement within the same low-power envelope of the VIA C7.

Initial production versions of the 1.0GHz VIA Nano ULV processor will have a maximum Thermal Design Power (TDP max) of just 5 watts (idle power of a mere 100mW), scaling up to 25 watts for the 1.8GHz VIA Nano processor with 500mW idle power.





3.6 VIA Padlock™ Security Engine

Recognizing the need for improved security, VIA has been working for many years to develop high-performance and affordable security features within its low power processors as part of a more holistic approach to information security. The VIA Nano Processor extends the VIA PadLock™ Security Engine into new areas of data protection, integrating various on-die building blocks designed to work in concert with secure communication, storage and e-commerce applications.

Taking on much of the heavy lifting associated with security programs, the VIA PadLock Security Engine aids demanding security applications without stressing system resources and affecting normal operation. This enables the development of small form factor, power efficient x86 consumer electronics and embedded devices that can be used for online entertainment associated with e-commerce and digital rights management.



Residing directly on the processor die, the VIA PadLock Security Engine is inherently more secure than software or chipset based security features that rely on vulnerable software drivers for operation. The VIA PadLock Security Engine comprises twin random number generators, AES encryption, NX bit, and Secure Hash Algorithms (SHA-1 and SHA-256).

3.6.1 VIA Padlock Random Number Generators

Random number generation is of paramount importance, forming the very basis of the encryption process. The source of the keys needed to secure information, and its entropy, largely dictates the strength of both symmetric and asymmetric encryption. Put simply, the stronger the keys, the stronger the level of security.

By harvesting random electrical oscillations on the surface of the die, VIA PadLock RNGs are capable of creating highly unpredictable random numbers at sustained rates of 12 million per second, depending on the quality of randomness required, fully addressing the needs of security applications requiring true randomness.

3.6.2 VIA Padlock Advanced Cryptography Engine

Chosen in the US as the government standard, AES encryption has been widely adopted due to the immensely complex computations required by its algorithm. Able to encrypt data at rates of up to 25 gigabits/sec (at 2GHz) - up to 200 times faster than a standard network connection – AES is used to securely stream information across an unsecured Internet connection, as well as to encrypt data in real time in order to stop hackers reading information on the drive.

3.6.3 NX Bit

This feature builds a virtual wall in system memory to prevent most worms from proliferating. By marking memory with an attribute that indicates that code should not be executed from that memory, NX bit helps to prevent damage or propagation of malicious code within x86 devices.



3.6.4 Secure Hash Algorithm

Secure Hash Algorithms are used in cryptography to provide message authentication codes (MAC) and digital signatures. These enable the recipient of information to verify the authenticity of the information's origin, and also that the information is correct. The VIA Nano provides two of the most commonly used, SHA-1 and SHA-256, which are able to encrypt information at rates of up to 5 gigabits/sec.

Table 2: Comparison of Security Features in Latest x86 Processors

	AMD Phenom	Intel Core 2	Intel Atom	VIA C7	VIA Nano
Secure Hash	No	No	No	Full SHA-1 & SHA-256	Full SHA-1 & SHA-256
Buffer Overflow	NX bit	NX bit	NX bit	NX bit	NX bit
On-die Encryption	No	No	No	Full AES en/decryption RSA acceleration CBC,CFB-M,AC, CTR modes 25Gb/s peak	Full AES encryption & decryption CBC,CFB-M,AC, CTR modes 25Gb/s peak
Random Number Generation (RNG)	No	No	No	2 Enhanced Hardware RNGs up to 12Mb/s Feeds output to SHA engine	2 Enhanced Hardware RNGs up to 12Mb/s Feeds output to SHA engine





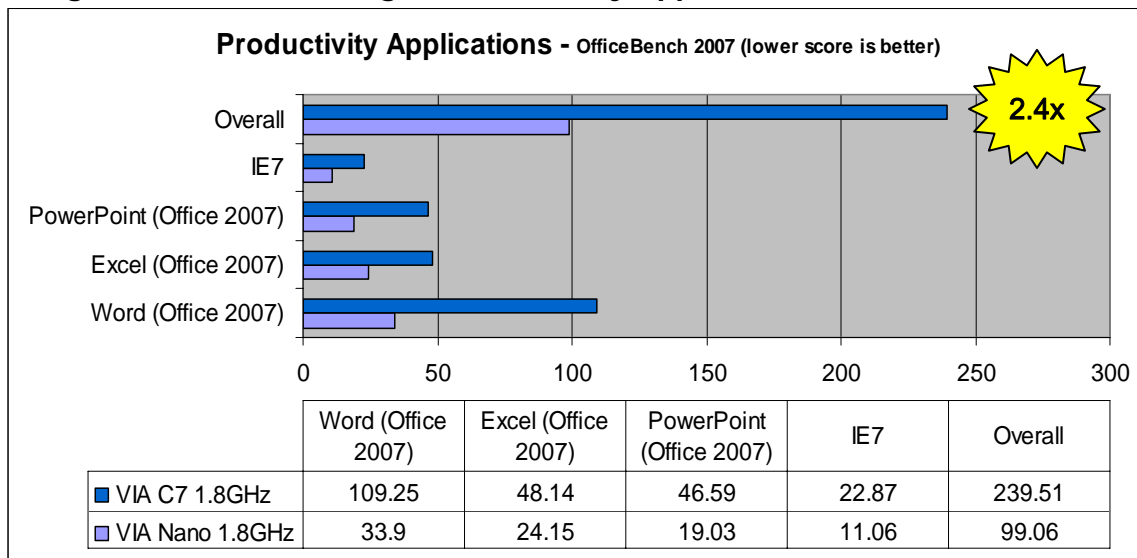
4. Performance

The following sections present benchmark results for the VIA Nano processor when matched with the popular VIA C7 processor. The comparative performance of the processors coupled with the new VIA VX800 digital media IGP chipset was tested with a variety of software applications grouped into three broad areas: productivity, multimedia and synthetics.

4.1 Productivity Applications

The VIA Nano processor offers performance increases of over 3 times on key productivity software applications.

Figure 4: Benchmarking of Productivity Applications

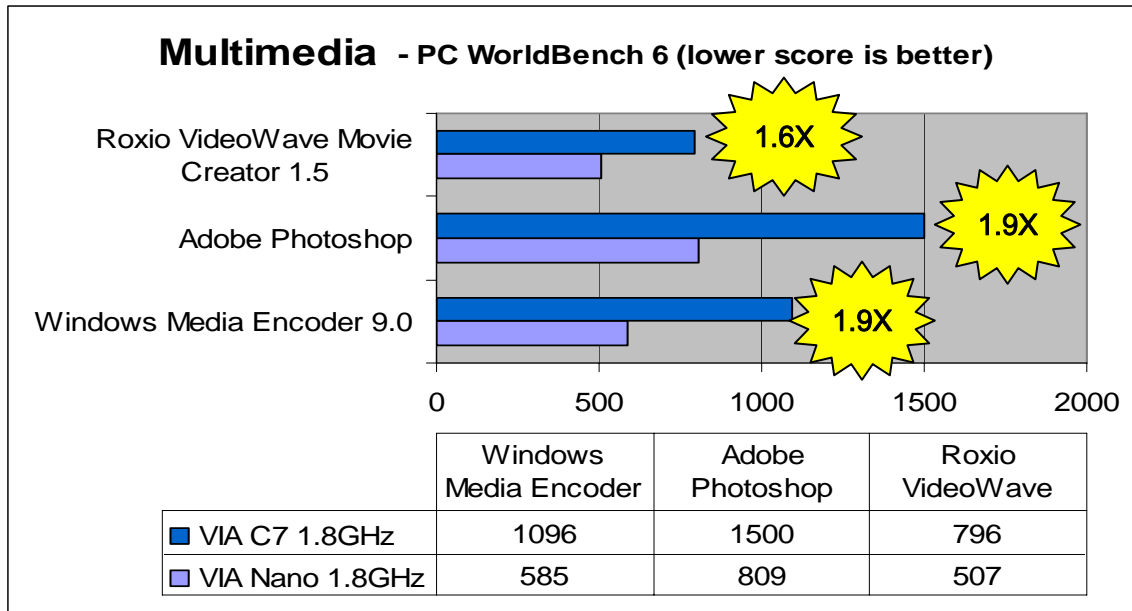




4.2 Multimedia

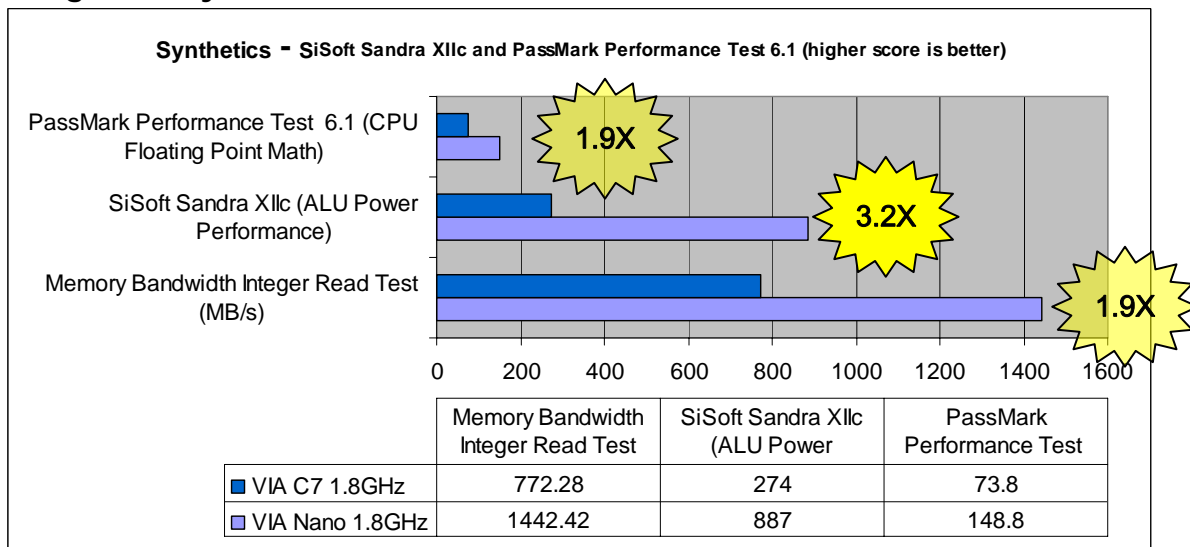
With the increasing importance of multimedia performance to contemporary computing, the VIA Nano processor's significant improvement over the VIA C7 opens the door to enhanced levels of usability and a superior user experience.

Figure 5: Benchmarking of Multimedia Applications



4.3 Synthetics

Figure 6: Synthetic Benchmarks



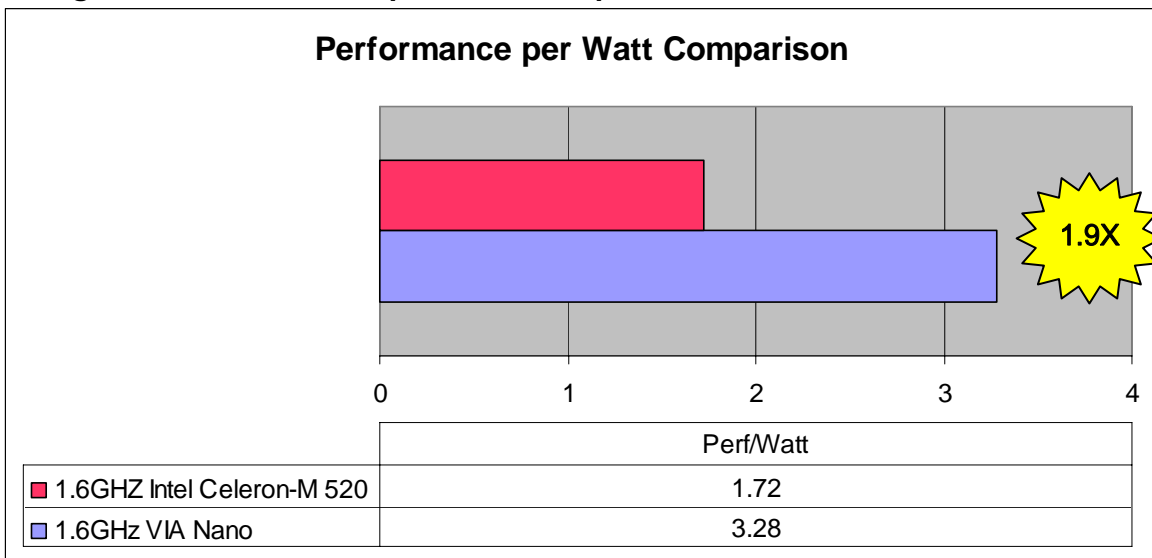


5. Performance per Watt

Since the introduction of the VIA C3[®] processor in 2001, VIA has led the industry in the design of power efficient x86 processor platforms. From desktops and laptops to thin clients and industrial computing systems, VIA processor platforms have built a reputation for leading performance per watt and cool operation.

Now, with the launch of the VIA Nano processor, VIA has raised the bar again. By keeping the same ultra low power envelope as previous VIA processors, while significantly improving on computing performance, the VIA Nano processor is easily the leading processor in terms of performance per watt on the market.

Figure 7: Performance per Watt Comparison



- Performance statistic based on overall score on OfficeBench 2007
- TDP for 1.6GHz Celeron-M = 31 watts; TDP for 1.6GHz VIA Nano = 17 watts
- OS = Windows Vista Enterprise



6. Conclusion

The VIA Nano processor has been designed to satisfy the needs of mainstream users and applications whilst also providing industry-leading efficiency in terms of both performance per dollar, and performance per watt. With its next-generation instruction set and the newest advances in processor architecture, the VIA Nano processor is uniquely suited to the rigorous computational and media processing demands of today's ICT devices.

With its focus on power efficient performance, the VIA Nano processor is poised to advance the growth of the notebook PC market, and to revitalize the traditional desktop PC segment with an exciting new range of small form factor systems, optimized for purpose.

7. Contacts

For more information on the VIA Nano processor, please contact Richard Brown, VIA Technologies, Inc, or CJ Holthaus, Centaur Technology, or access the VIA corporate website at www.viatech.com.

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